

This cross-sectional view shows a substrate 100 with a thin layer 110 on top. A thicker layer 115 is deposited over layer 110. On top of layer 115, there are two raised regions 120, each containing a central portion 126. A gap 122 is formed between these two raised regions. The top surface of the raised regions 120 is indicated by a dashed line.

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FIG. 4
(PRIOR ART)

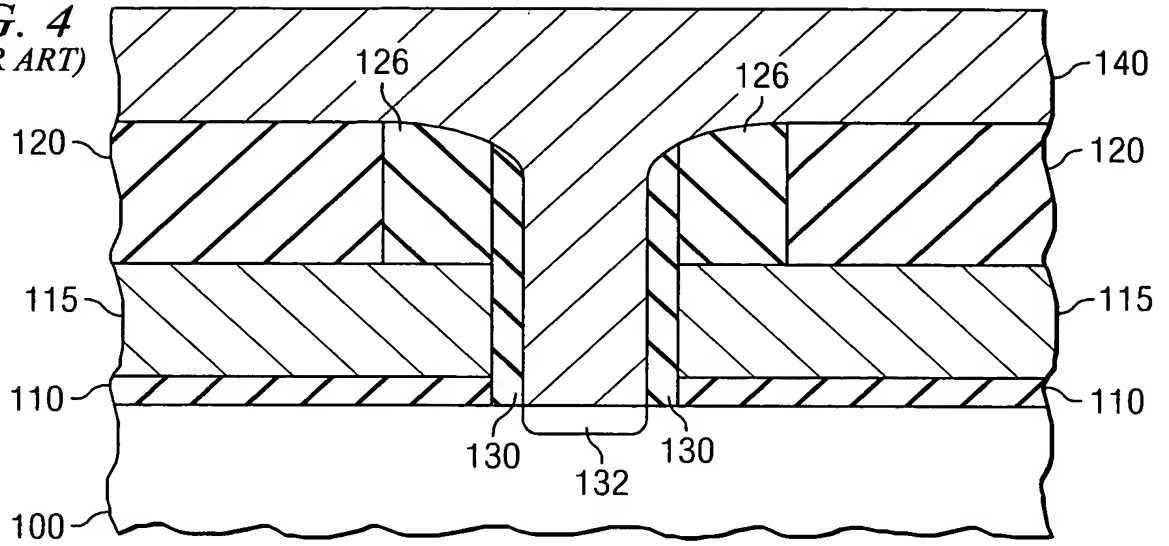


FIG. 5
(PRIOR ART)

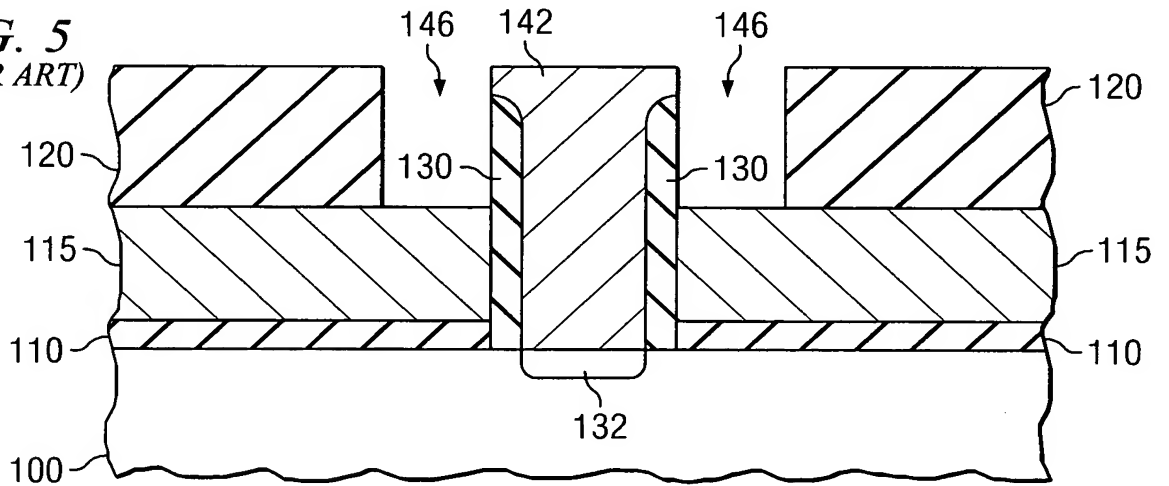


FIG. 6
(PRIOR ART)

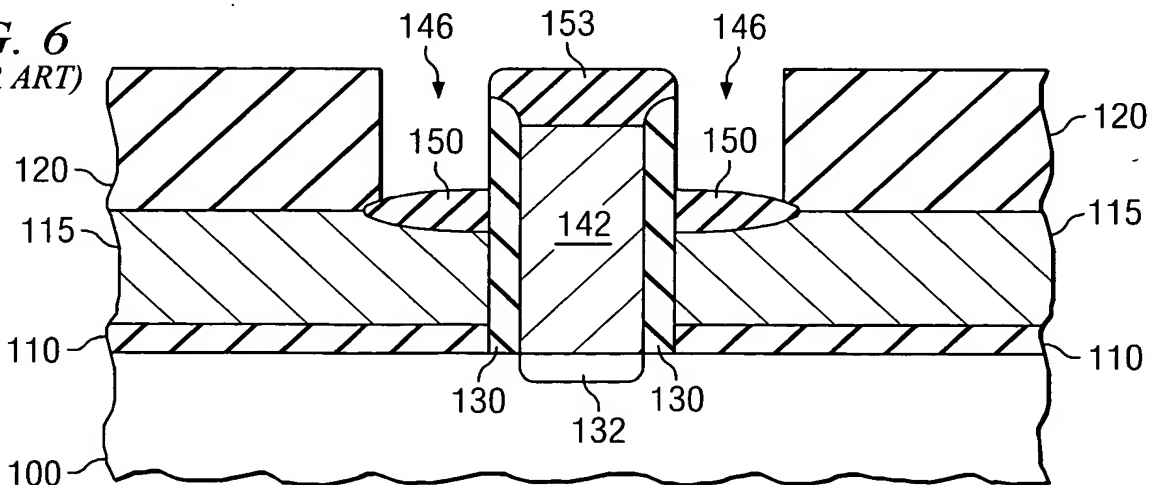


FIG. 7
(PRIOR ART)

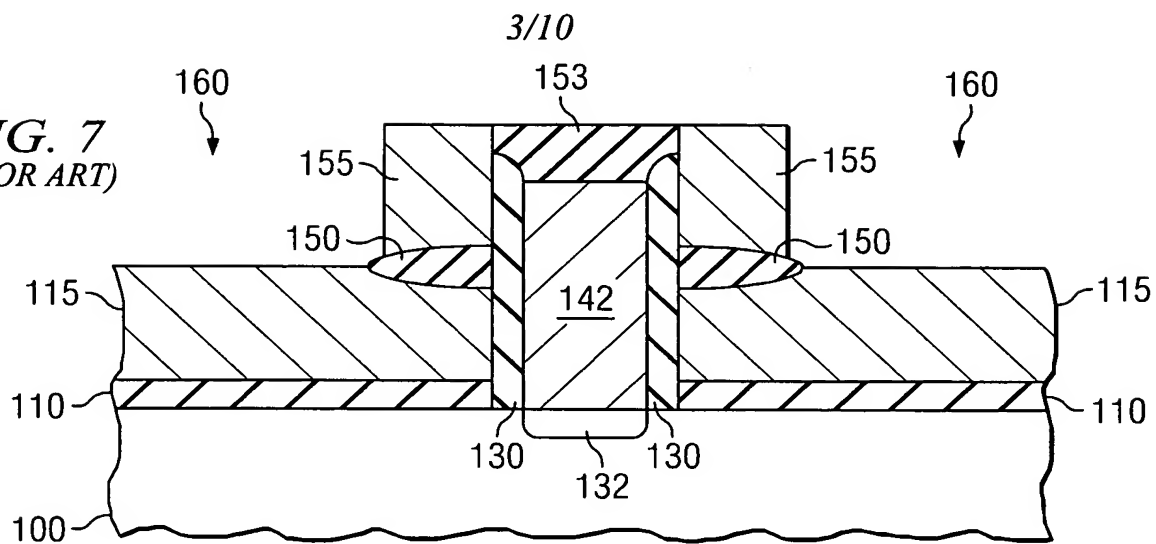


FIG. 8
(PRIOR ART)

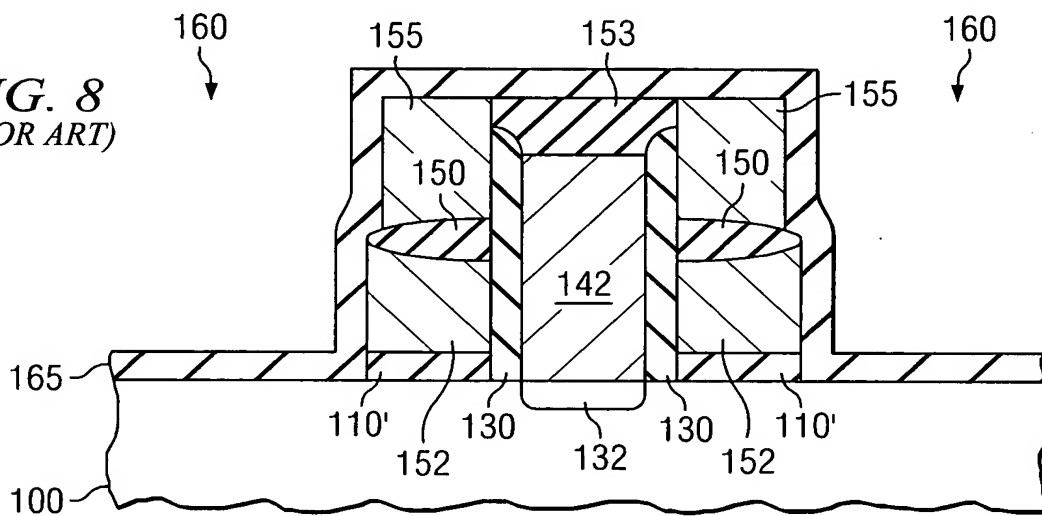


FIG. 9
(PRIOR ART)

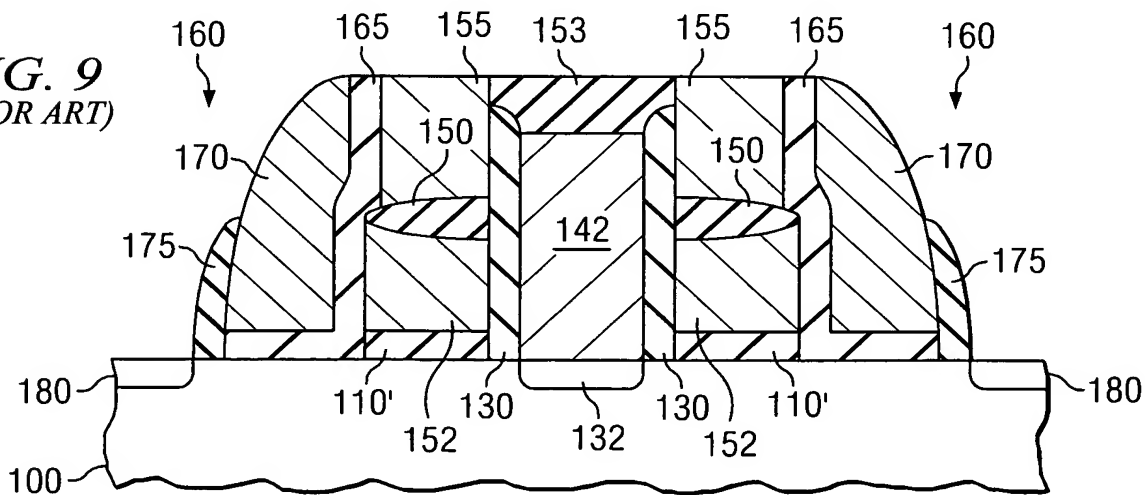
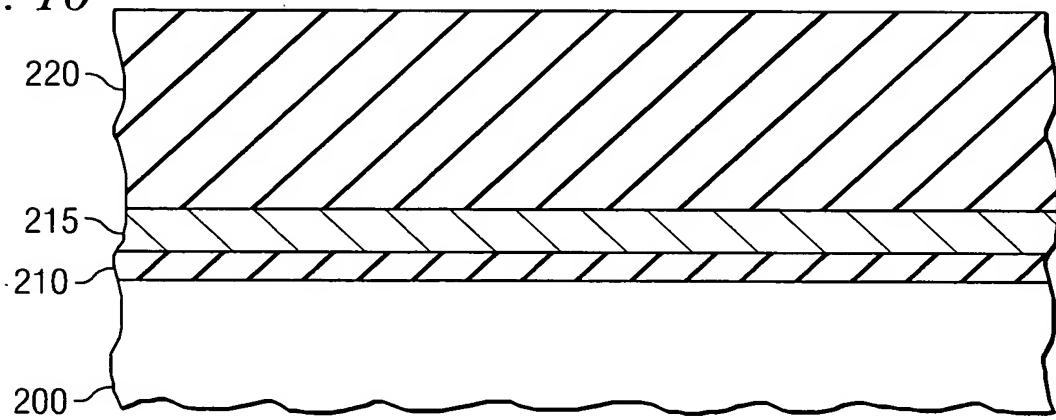
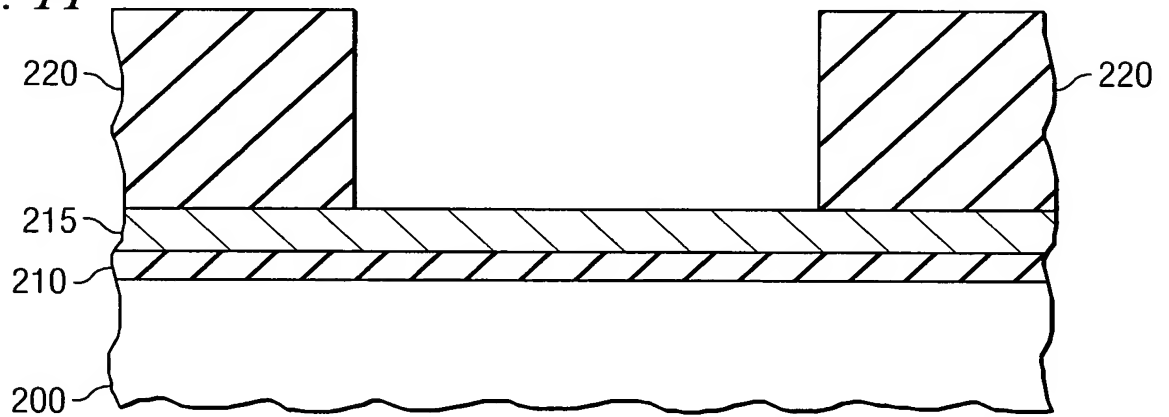
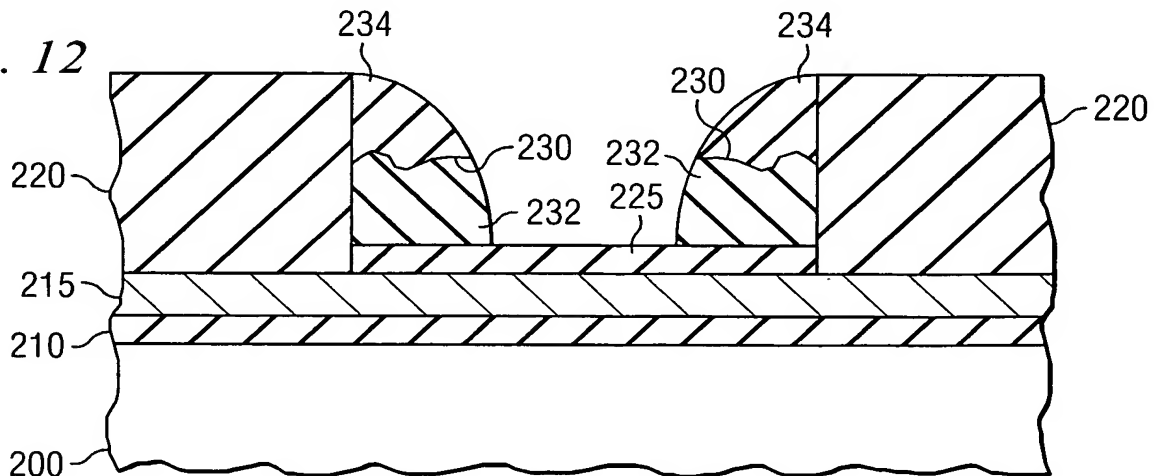
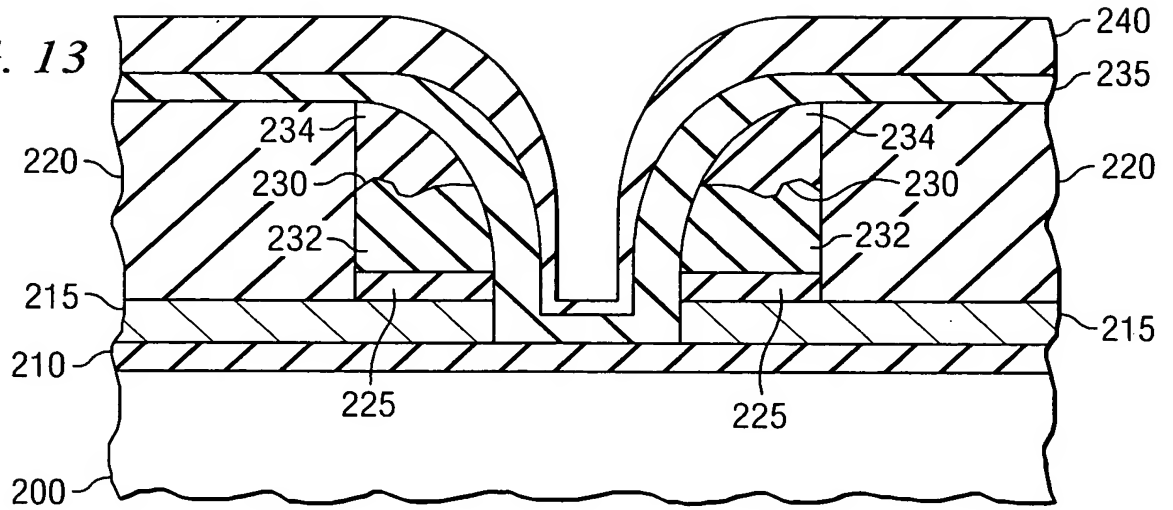
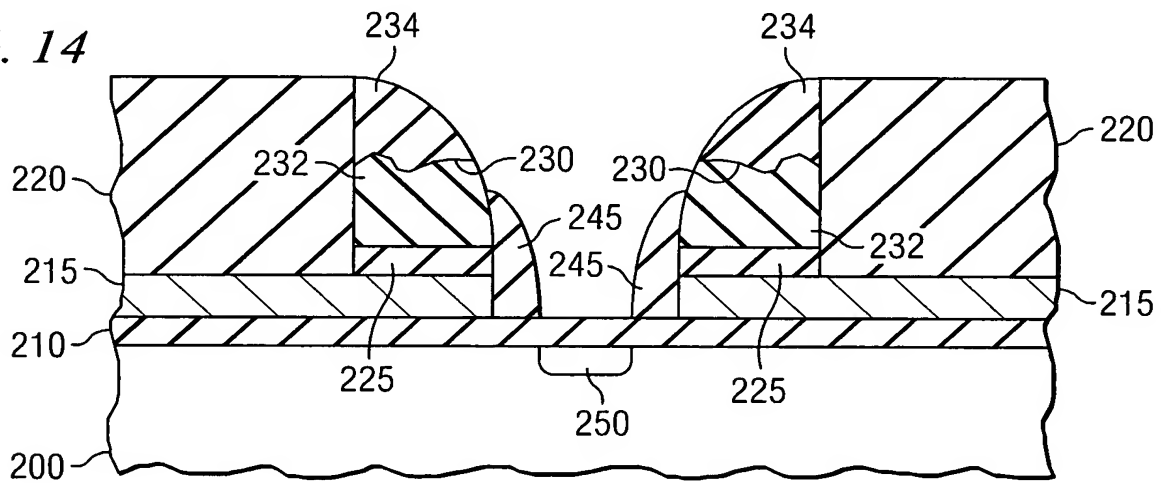
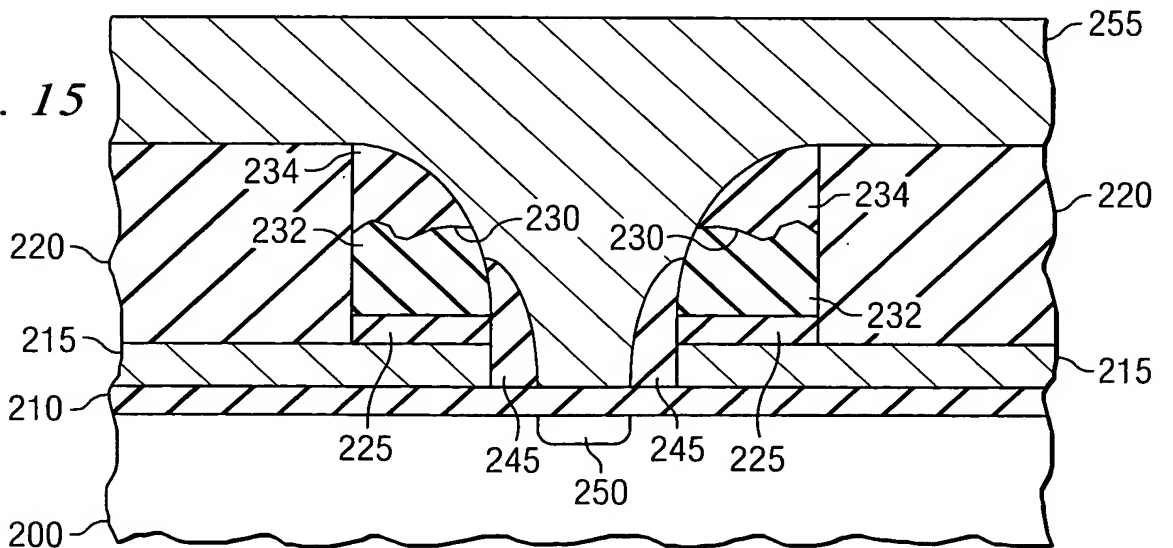


FIG. 10*FIG. 11**FIG. 12*

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FIG. 13*FIG. 14**FIG. 15*

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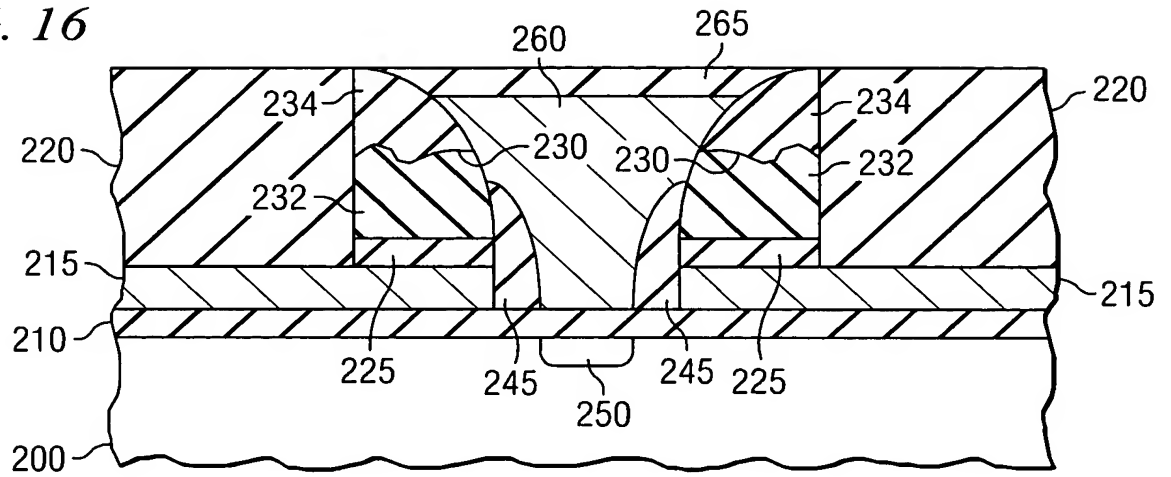
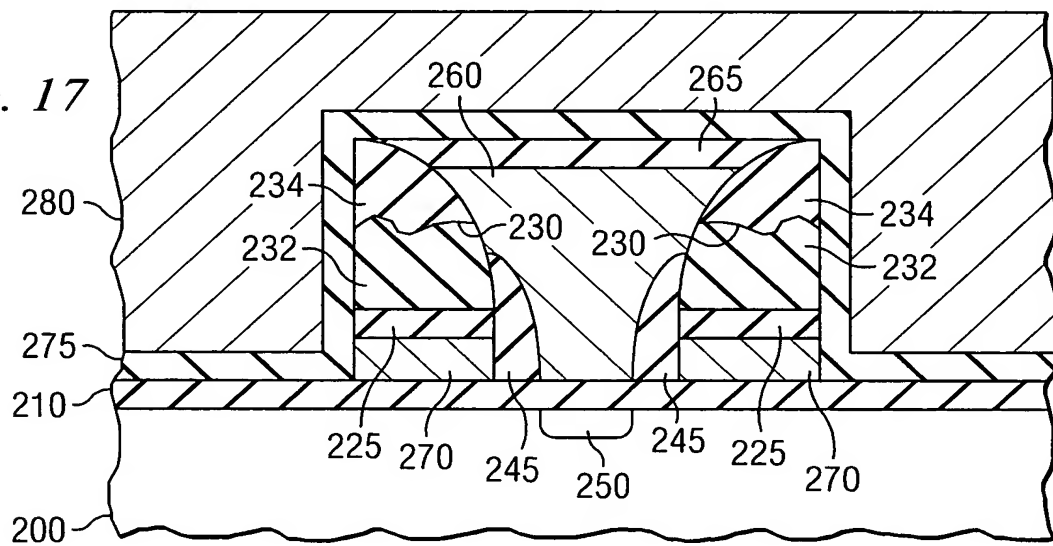
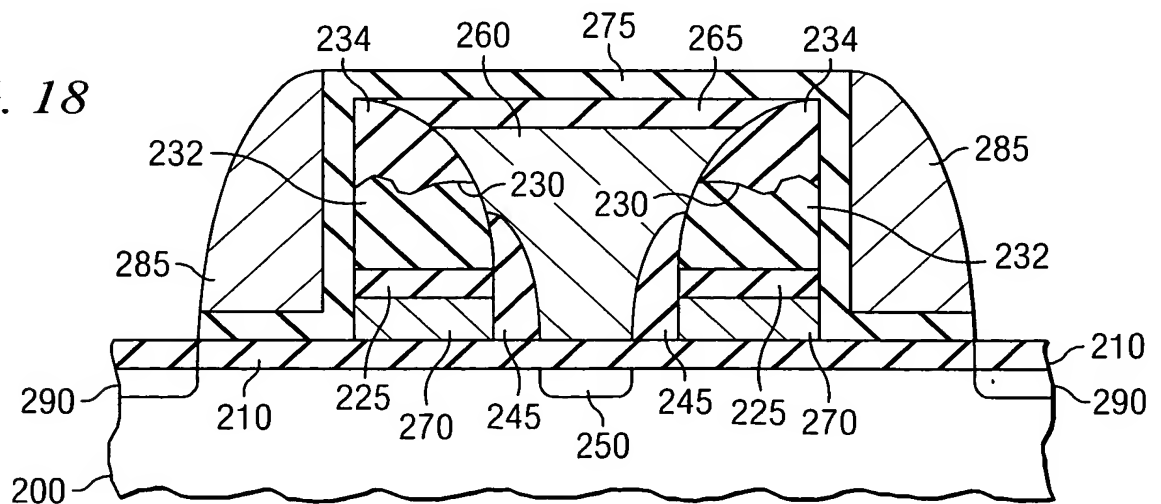
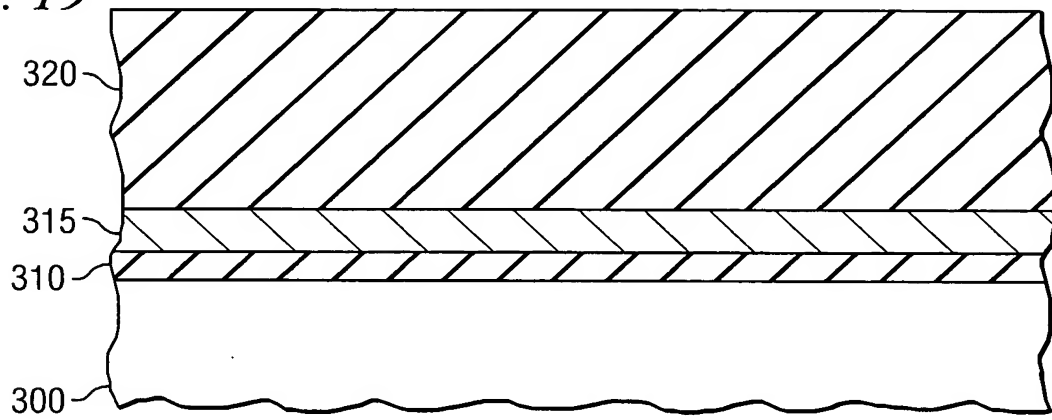
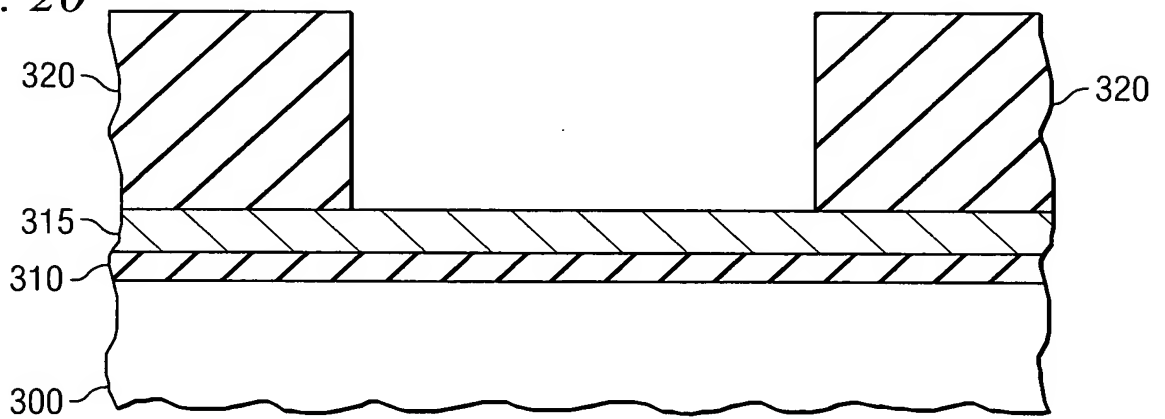
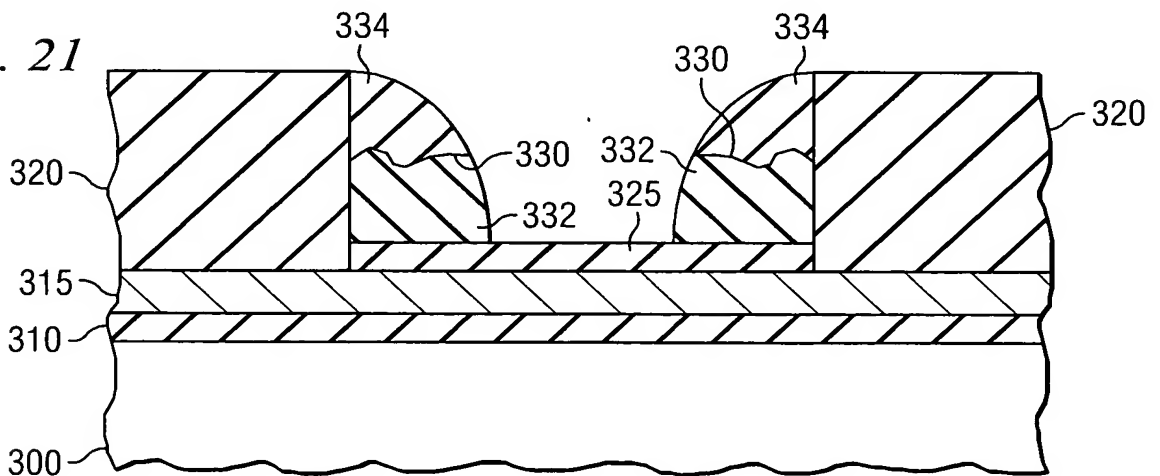
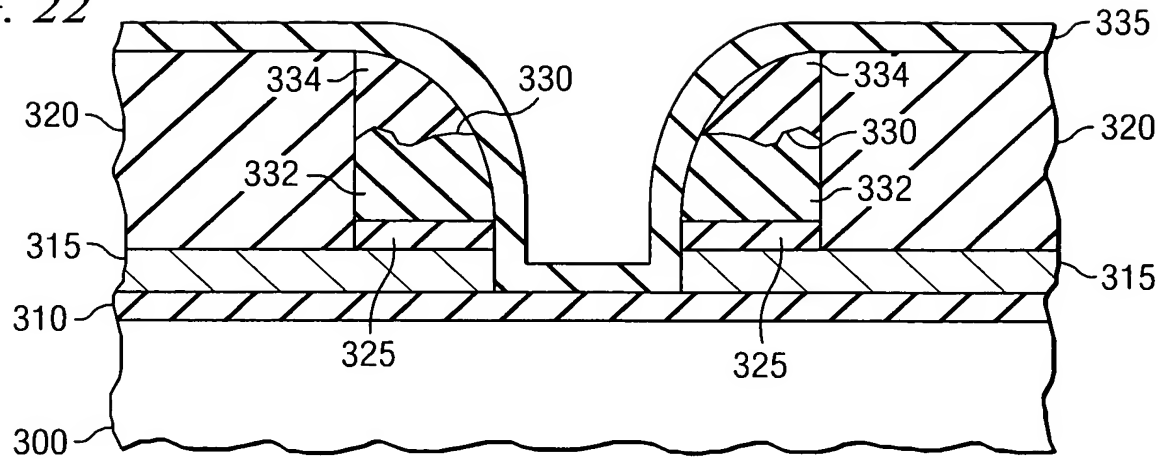
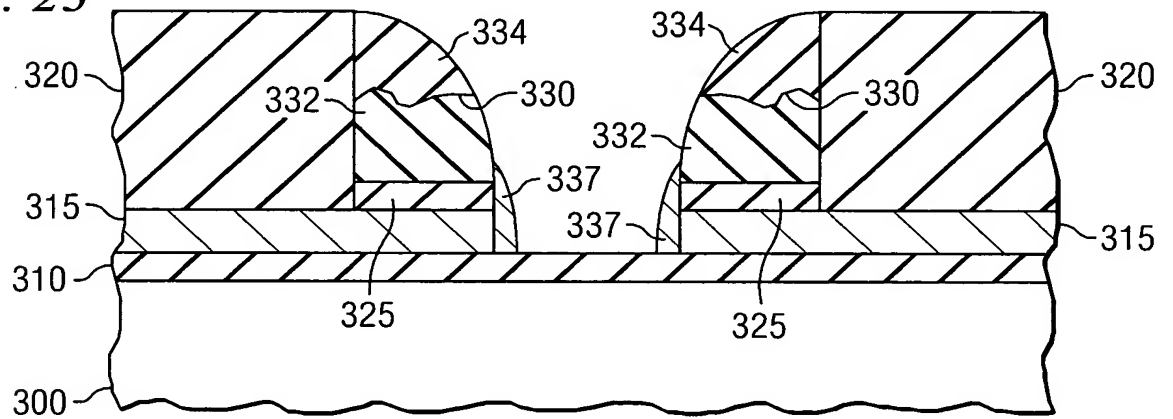
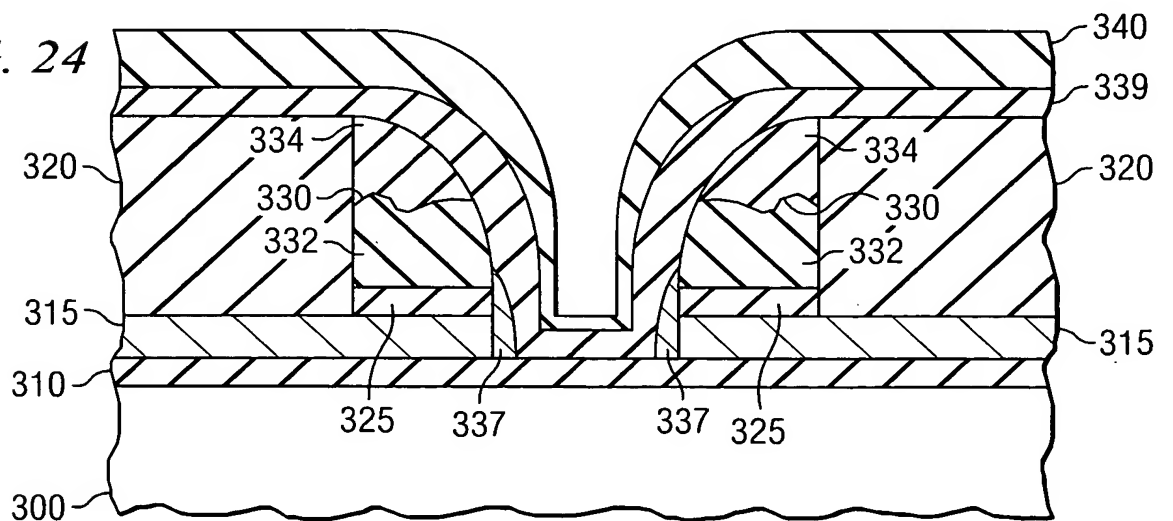
FIG. 16**FIG. 17****FIG. 18**

FIG. 19*FIG. 20**FIG. 21*

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FIG. 22**FIG. 23****FIG. 24**

This cross-sectional view shows two semiconductor elements, 320, positioned on a substrate 300. Each element 320 includes a top layer 334, a middle layer 332, and a bottom layer 330. A thin layer 315 is located between the middle layer 332 and the bottom layer 330. A layer 325 is situated between the two semiconductor elements 320. A layer 310 is located between the middle layer 332 and the layer 325. A layer 337 is located between the bottom layer 330 and the layer 325. A layer 345 is located between the middle layer 332 and the bottom layer 330. A layer 350 is located between the bottom layer 330 and the layer 325.

Figure 27 is a cross-sectional view of a semiconductor device 27. The device includes a substrate 300, a base layer 310, and a first conductive layer 315. A second conductive layer 320 is formed on the first conductive layer 315. The second conductive layer 320 includes a central region 330 and side regions 332. The side regions 332 are separated from the central region 330 by a gap 334. The second conductive layer 320 is formed on a dielectric layer 325. The dielectric layer 325 is formed on the base layer 310. The dielectric layer 325 includes a central region 337 and side regions 337. The side regions 337 are separated from the central region 337 by a gap 334. The dielectric layer 325 is formed on a base layer 310. The base layer 310 is formed on a substrate 300. The substrate 300 is a semiconductor material. The device 27 is a semiconductor device.

[illegible]

Figure 29 is a cross-sectional view of a semiconductor device 29. The device features a substrate 300 with a base layer 310. A central region 330 is defined by a top layer 334 and a bottom layer 332. This central region is flanked by side regions 335. The top layer 334 is composed of a material 360 and a material 375. The bottom layer 332 is composed of a material 345 and a material 370. The side regions 335 are composed of a material 385. The device is further defined by a top layer 390 and a bottom layer 350. The central region 330 is further divided into sub-regions 337 and 325.